Amendments to the Specification:

Please replace paragraph [0004] with the following amended paragraph:

In certain application of IC technology, situations might ~~come across~~ occur where a different power supply voltage is required for operating in different modes, such as non-volatile flash memory. In prior art, a power supply voltage switch circuit is often used to accomplish the switching of different power supply ~~voltage~~ voltages in different operating modes.

Please replace paragraph [0008] with the following amended paragraph:

In the above-mentioned configuration, the power supply voltage switching circuit 10 can generate a power supply voltage V_{PS} from the first voltage V_{PP} and the second voltage V_{DD} according to the control of the first control signal ENVPP and the second control signal ENVDD. If the first voltage V_{PP} is chosen to be the power supply voltage V_{PS}, the control circuit sets the first control signal ENVPP to a logic value of 0 (i.e. 0V) and the second control signal ENVDD to a logic value of 1 (i.e. 3V). After the level shift by the level shifting module 12, the first control signal ENVPP remains 0V but the second control signal ENVDD becomes 7V, and both are inputted to the selecting switch module 18. At the same time, the first voltage V_{PP} is 7V and the second voltage V_{DD} is 3V so the third p-type MOS transistor 20 is ~~in conduct~~ switched on and the fourth p--type MOS transistor 22 is switched off. As a result the power supply voltage V_{PS} will output the value of the first voltage V_{PP} (i.e. 7V). Oppositely if the second voltage V_{DD} is chosen to be the power supply voltage V_{PS}, the control circuit sets the first control signal ENVPP to a logic value of 1 (i.e. 3V) and the second control signal ENVDD to a logic value of 0 (i.e. 0V). After the level shift by the level shifting module 12, the first control signal ENVPP becomes 7V but the second control signal ENVDD remains 0V, and both are inputted to the selecting switch module 18. At the same time, the first voltage V_{PP} is 7V and the

second voltage V_{DD} is 3V so the third p-type MOS transistor 20 is switched off and the fourth p-type MOS transistor 22 is ~~in conduct~~ switched on. As a result the power supply voltage V_{PS} will output the value of the second voltage V_{DD} (i.e. 3V).

Please replace paragraph [0009] with the following amended paragraph:

Furthermore, the above operation takes into the assumption that the value of the first voltage V_{PP} does not change. However in certain ~~design of~~ circuits, it is possible that the value of the first voltage V_{PP} cannot always be maintained at a charge-pumped level, an example is the sharing of a pad between a charge-pumped voltage (such as V_{PP}) and other signals. In this condition, the value of the first voltage V_{PP} can be at a comparatively low level or even become 0V or floating in some ~~situation~~ situations. The level-shifters 14 and 16 of the level shifting module 12 use the first voltage V_{PP} as the power supply voltage which renders the selecting switch module 18 unable to operate properly, or renders the third and fourth p-type MOS transistors 20 and 22 to be ~~in conduct~~ switched on at the same time causing the first voltage V_{PP} and the second voltage V_{DD} to short circuit which wastes energy.

Please replace paragraph [0012] with the following amended paragraph:

The claimed invention discloses a high voltage selecting circuit comprising: a first transistor where a first terminal of the first transistor ~~being~~ is electrically coupled to a first voltage, a second terminal of the first transistor ~~being~~ is electrically coupled to an output junction, and a gate of the first transistor ~~being~~ is electrically coupled to a second voltage; and a second transistor where a first terminal of the second transistor ~~being~~ is electrically coupled to the second voltage, a second terminal of the second transistor ~~being~~ is electrically coupled to the output junction, and a gate of the second transistor ~~being~~ is electrically coupled to the first voltage; wherein the high voltage selecting circuit

selectively generates an output voltage according to a higher one of the first voltage and the second voltage.

Please replace paragraph [0021] with the following amended paragraph:

Under the configuration of the high voltage selecting module 44 in this embodiment, if the absolute value of the difference between the first voltage V_{PP} and the second voltage V_{DD} is greater than the threshold voltage V_{TH} of the transistors 46, 48, the voltage difference between the source and the gate will be greater than the threshold voltage so the channel is ~~in conduct~~ conducting, therefore the output voltage VV is substantially the greater one of the first voltage V_{PP} and the second voltage V_{DD}. If the absolute value of the difference between the first voltage V_{PP} and the second voltage V_{DD} is smaller than or equal to the threshold voltage V_{TH} of the transistors 46, 48, in view of the fact that the wells of the transistors 46, ~~48are~~ 48 are respectively electrically coupled to the drain of the transistors 46, 48, although the channel is not ~~in conduct~~ conducting due to the difference between the source and the gate being smaller than or equal to the threshold voltage[[,]]. ~~because~~ Because of the existence of a PN junction between the source and the well (i.e. the drain), the output voltage VV is substantially the higher one of the first voltage V_{PP} and the second voltage V_{DD} minus the junction voltage V_D that is between the source and the well (i.e. the diode voltage of an equivalent diode formed by the source and the well).

Please replace paragraph [0024] with the following amended paragraph:

The power supply voltage of the level-shifters 34 and 36 is 3V so when the first voltage V_{PP} is to be chosen as the power supply voltage V_{PS} the control circuit will set the logic value of the first control signal ENVPP to 0 (i.e. 0V) and the logic value of the second control signal ENVDD to 1 (i.e. 3V). After the level-shifting by the level shifting

module 32, the first control signal ENVPPHV will be 0V and the second control signal ENVDDHV will be 3V and they are inputted to the selecting switch module 38. At this time, the first voltage V_{PP} is 1V and the second voltage V_{DD} is 3V so the third p-type MOS transistor 40 is switched on and the fourth p-type MOS transistor 42 is switched off. As a result, the power supply voltage V_{PS} is the first voltage V_{PP} (being 1V). Oppositely when the second voltage V_{DD} ~~power supply voltage V_{PS}~~ is to be chosen as ~~the second voltage V_{DD}~~ power supply voltage V_{PS}, the control circuit will set the logic value of the first control signal ENVPP to 1 (i.e. 3V) and the logic value of the second control signal ENVDD to 0 (i.e. 0V). After the level-shifting by the level shifting module 32, the first control signal ENVPPHV will be 3V and the second control signal ENVDDHV will be 0V and they are inputted to the selecting switch module 38. At this time, the first voltage V_{PP} is 1V and the second voltage V_{DD} is 3V so the third p-type MOS transistor 40 is switched off and the fourth p-type MOS transistor 42 is switched on. As a result, the power supply voltage V_{PS} is the second voltage V_{DD} (being 3V).

Please replace paragraph [0025] with the following amended paragraph:

Following assume the first voltage is 3.5V and the second voltage is 3V. In this situation, the first p-type MOS transistor 46 is switched off and the second p-type MOS transistor 48 is switched off. Thus, the output voltage VV equals the second voltage V_{DD} minus V_D, that is 3.5V-0.65V=2.85V because the first voltage V_{PP} is ~~in conduct with~~ connected to the output node through the PN junction that is formed between the source and the well.